are suppressed because these dopants, present in the overlying metal, metal silicide, or metal nitride film **24**, cannot cross the UBDBL **28** and enter the N+ polysilicon layer **21**.

Finally, in the embodiment illustrated in Fig. 7, the UBDBL **28** is formed in the polysilicide gate electrode structure over the N+ polysilicon layer **21** and the P+ polysilicon layer **22**. In this manner, migration of P+ dopants from the P+ polysilicon layer **22** and migration of N+ dopants from the N+ polysilicon layer **21** to the overlying metal, metal silicide, or metal nitride film **24** is significantly impeded by the UBDBL **28**. Cross diffusion and gate depletion are suppressed because the dopants cannot cross the UBDBL **28** and enter the opposite polysilicon layer.--

IN THE ABSTRACT

Please replace the ABSTRACT OF THE DISCLOSURE, with:

--According to the present invention, an ultrathin buried diffusion barrier layer (UBDBL) is formed over all or part of the doped polysilicon layer of a polysilicide structure composed of the polycrystalline silicon film and an overlying film of a metal, metal silicide, or metal nitride. More specifically, according to one embodiment of the present invention, a memory cell is provided comprising a semiconductor substrate, a P well, an N well, an N type active region, a P type active region, an isolation region, a polysilicide gate electrode structure, and a diffusion barrier layer. The P well is formed in the semiconductor substrate. The N well is formed in the semiconductor substrate adjacent to the P well. The N type active region is defined in the P well and the P type active region is defined in the N well. The isolation region is arranged to isolate the N type active region from the P type active region. The polysilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer formed with the N type active region and a P+ polysilicon layer formed with the P type active region. The diffusion barrier layer is formed in the polysilicide gate electrode structure over a substantial portion of the polycrystalline silicon film between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film.--